REMARKS

This responds to the Office Action mailed on April 5, 2004.

Claims 1, 2, 4-9, 14, 16, 18, 20, 22 – 24, 26 – 29, 31, 33 – 36, 38, 40 – 43, 46,49, 52, 55, and 57 - 60 are amended. No claims are cancelled or added. As a result, claims 1 – 60 remain pending in this patent application.

Telephonic Interview

Applicant's counsel, Suneel Arora, thanks Examiner Trong Phan for the helpful telephonic interview on June 24, 2004. No claims or references were discussed. The only point discussed during the telephonic interview was clarification of the following language in the Office Action mailed on April 5, 2004:

> Claims 1-12 and 14-60 are not understood because the feature of "the first and second banks interleaved in each row in an alternating fashion" is not shown in the drawings of the present invention. As shown in Fig. 3 of the present invention, each bank 0 is interconnected with each bank 1 along each row direction (horizontal axis) via each shared sense amplifier. Therefore, it is not understood that what the alternating fashion really is.

(Office Action ¶ 3.) During the telephonic interview, the differences between Applicant's FIG. 1 (labeled "Prior Art") and FIG. 3 were discussed. Applicant explained the differences between these figures by noting that the top row of FIG. 3 (from right-to-left) shows Bank 0, Bank 1, Bank 0, Bank 1, Bank 0, Bank 1, etc. memory core blocks interleaved in alternating fashion, while the top row of FIG. 1 (from right-to-left) merely shows memory core blocks from Bank 0, Bank 1, Bank 2, Bank 3, Bank 4, . . . , up to Bank (n-1)—that is, the Banks are not interleaved in alternating fashion in FIG. 1. This is because, among other things, no row in FIG. 1 includes at least two memory cores from the same memory bank. Therefore FIG. 1 cannot obtain an alternating or interleaved arrangement. No agreement was reached during the telephonic interview.

§112 Rejection of the Claims

Claims 1-12 and 14-60 were rejected under 35 U.S.C. § 112, first paragraph, as lacking adequate enablement. Applicant respectfully traverses.

The Office Action states:

> Claims 1-12 and 14-60 are not understood because the feature of "the first and second banks interleaved in each row in an alternating fashion" is not shown in the drawings of the present invention. As shown in Fig. 3 of the present invention, each bank 0 is interconnected with each bank 1 along each row direction (horizontal axis) via each shared sense amplifier. Therefore, it is not understood that what the alternating fashion really is.

(Office Action ¶ 3.) However, the top row of FIG. 3 (from right-to-left) clearly shows Bank 0, Bank 1, Bank 0, Bank 1, Bank 0, Bank 1, etc. blocks interleaved in alternating fashion. Therefore, Applicant respectfully submits that FIG. 3 of the present specification clearly enables any claims reciting that blocks from such Banks are "interleaved," "alternating," "every other," or similar language. That is, Bank 0 and Bank 1 blocks are physically located in alternating or interleaved fashion. Therefore, Applicant submits that FIG. 3 does provide adequate enablement for such claims, and accordingly Applicant respectfully requests withdrawal of this basis of rejection of those claims including such language.

Moreover, in response to the Office Action's statement that "As shown in Fig. 3 of the present invention, each bank 0 is *interconnected* with each bank 1 along each row direction (horizontal axis) via each shared sense amplifier" (Office Action ¶ 3 (emphasis added)), Applicant notes that this statement fails to rebut the *interleaving* of blocks from Bank 0 and Bank 1 as clearly depicted in FIG. 3. The Office Action appears to be interpreting the term "interleaved" as identical in meaning to the term "interconnected." This is simply not the case. Applicant respectfully submits that the term "interleaved" means arranged in an alternating sequence (e.g., Bank 0, Bank 1, Bank 0, Bank 1, etc.), which is not shown in FIG. 1. By contrast the term "interconnected" does not connote an alternating sequence. Therefore, Applicant respectfully objects to the Office Action's confounding these two terms in its analysis.

Also in response to the Office Action's statement that "As shown in Fig. 3 of the present invention, each bank 0 is *interconnected* with each bank 1 along each row direction (horizontal axis) via each shared sense amplifier" (Office Action ¶ 3 (emphasis added)), Applicant notes that

although the various blocks from Bank 0 and Bank 1 share common column decode lines (*see* Specification at page 6, lines 13 – 14), every block in the row is not necessarily functionally interconnected with every other block in the row via every shared sense amplifier, as asserted in the Office Action. Instead, each sense amplifier services only those block(s) to which it is adjacent. Therefore, Applicant respectfully submits that this remark in the Office Action is mistaken and, accordingly, Applicant further requests that this remark specifically be withdrawn.

Applicant has amended the claims to more clearly define what exactly constitutes a bank of memory cores. Applicant notes that the claims now recite or incorporate language explaining that a bank of memory cores is selectable to activate or deactivate all of the memory cores in the bank together as a group. Support for this amendment is found in the specification of the present application. (*See, e.g.,* Specification at page 1, lines 16 – 18 and 25, and page 6, line 21 to page 7, line 10.)

§103 Rejection of the Claims

Claims 1-12 and 14-60 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's Fig. 1 labeled "Prior Art." Applicant respectfully traverses on the grounds that no *prima facie* case of obviousness exists with respect to the claims, because all elements in the claims are not disclosed, taught, or suggested in Applicant's Fig. 1 labeled "Prior Art."

Regarding claims 1 – 4:

Applicant cannot find in Fig. 1, any disclosure, teaching, or suggestion of, among other things, a first one of the first strips including all memory core blocks from a first memory bank and all memory core blocks from a second memory bank, the memory core blocks from the first and second banks being interleaved in the first one of the first strips in an alternating fashion, as recited or incorporated in these claims. Instead, Fig. 1 shows rows with only one memory core block from each bank, with other memory core blocks from the same bank being in different rows. Moreover, Fig. 1 does not show interleaving in an alternating fashion, as discussed above. Accordingly, Applicant respectfully requests withdrawal of this basis of rejection of these claims.

Regarding claims 5 – 8:

Applicant cannot find in Fig. 1, any disclosure, teaching, or suggestion of, among other things, memory cores in a first one of the first strips are arranged in an alternating fashion of two different banks, and each memory core in a first one of the second strips being associated with a different one of the banks, as recited or incorporated in these claims. Neither the rows or columns in Fig. 1 have memory cores alternating between two different banks (e.g., Bank 0, Bank 1, Bank 0, Bank 1, etc.). Moreover, the columns in Fig. 1 have memory cores all associated with the same Bank, rather than with different banks, as recited or incorporated in these claims. Accordingly, Applicant respectfully requests withdrawal of this basis of rejection of these claims.

Regarding claims 9 – 12:

Applicant cannot find in Fig. 1, any disclosure, teaching, or suggestion of, among other things, first and second banks of memory cores interleaved in a linear strip, the strip comprising only those memory cores from the first and second banks, as recited or incorporated in these claims. Fig. 1 fails to disclose interleaving, as discussed above. Fig. 1 also fails to disclose using only those memory cores from the first and second banks—for example, the top row of Fig. 1 shows memory cores from many (e.g., "n") banks. Accordingly, Applicant respectfully requests withdrawal of this basis of rejection of these claims.

Regarding claims 14 – 35 and 43-45:

Applicant cannot find in Fig. 1, any disclosure, teaching, or suggestion of, among other things, first and second banks of memory cores interleaved in a strip that includes all of the memory cores in the first and second banks, as recited or incorporated in these claims. Instead, all of the memory cores of a particular bank in Fig. 1 appear in the same column, without being interleaved in that same column with any memory cores from another bank. Accordingly, Applicant respectfully requests withdrawal of this basis of rejection of these claims.

Regarding claims 36 – 39:

Applicant cannot find in Fig. 1, any disclosure, teaching, or suggestion of, among other things, a memory device in which all of the memory cores are arranged in a first horizontal strip alternate between a first bank and a second bank, as recited or incorporated in these claims. Instead, the top row of Fig. 1 includes only one of the Bank 0 memory cores. The other Bank 0 memory cores do not appear in the top row of Fig. 1, but instead appear across a single column of Fig. 1 that includes numerous other rows. Accordingly, Applicant respectfully requests withdrawal of this basis of rejection of these claims.

Regarding claims 40 – 42:

Applicant cannot find in Fig. 1, any disclosure, teaching, or suggestion of, among other things, a memory device in which all of the memory cores arranged in a first horizontal strip alternate between a first bank and a second bank, and in which column decode conductors arranged in the first horizontal strip to cross memory cores from only the first bank and the second bank, as recited or incorporated in these claims. Instead, in Fig. 1, all of the memory cores in the top row (for example) are drawn from many different banks (e.g., Bank 0, Bank 1, Bank 2, Bank 3, . . ., Bank (n-1)) without any alternation (or even duplication of more than one memory core from the same bank). Likewise, the column decode conductors in Fig. 1 do not traverse memory cores from only two banks, but instead traverse memory cores from many different banks (e.g., Bank 0, Bank 1, Bank 2, Bank 3, . . ., Bank (n-1)). Accordingly, Applicant respectfully requests withdrawal of this basis of rejection of these claims.

Regarding claims 46 – 48:

Applicant cannot find in Fig. 1, any disclosure, teaching, or suggestion of, among other things, only every other memory core within a first horizontal strip that is assigned to the same bank, and wherein each of the memory cores in the first horizontal strip are associated with one of only two of the banks, as recited or incorporated in these claims. Instead, the top row (for example) of Fig. 1 does not even include more than one memory core from the same memory bank, therefore, it cannot possibly show every other memory core within the top row being assigned to the same bank. Neither can any column in Fig. 1 meet this claim language. For example, the right-most column in Fig. 1 shows all memory cores associated with the same memory bank, therefore, it does not meet the requirement that "only" every other memory core within the strip be assigned to the same bank. Likewise, the top row of Fig. 1 shows memory cores associated with more than two banks, therefore, it fails to meet the claim language stating that each of the memory cores in the first horizontal strip are associated with one of only two of the banks. Moreover, each column in Fig. 1 fails to meet the claim language that two of the banks are represented by memory cores in the first horizontal strip, since each column in Fig. 1 includes only memory cores from a single memory bank. Accordingly, Applicant respectfully requests withdrawal of this basis of rejection of these claims.

Regarding claims 49 – 51:

Applicant cannot find in Fig. 1, any disclosure, teaching, or suggestion of, among other things, first and second banks of memory cores interleaved together in a first horizontal strip, wherein all of the memory cores in the first and second banks are located in the first horizontal strip, and third and fourth banks of memory cores interleaved together in a second horizontal strip, wherein all of the memory cores in the third and fourth banks being located in the second horizontal strip, as recited or incorporated in these claims. Instead, all of the memory cores of a particular bank in Fig. 1 appear in the same column, without being interleaved in that same column with any memory cores from another bank. No horizontal or vertical strip in Fig. 1 includes all memory cores associated with a particular bank interleaved with all memory cores associated with a different bank. Accordingly, Applicant respectfully requests withdrawal of this basis of rejection of these claims.

Regarding claims 52 – 60:

Applicant cannot find in Fig. 1, any disclosure, teaching, or suggestion of, among other things, all of the memory cores of the first bank and all of the memory cores of the second bank being arranged in a strip, or similar language as recited or incorporated in these claims. Instead, each row of Fig. 1 shows only one memory core from each bank, with the other memory cores from that bank spread out over a column that includes all of the other rows. Likewise, each column of Fig. 1 includes only all memory cores from a first bank, and fails to include any memory cores from a second bank. Accordingly, Applicant respectfully requests withdrawal of this basis of rejection of these claims.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612) 373-6904 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date July 6, 2004

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 6th day of July, 2004.

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Signature _____